In re Patent Application of: Takuya Sugawara et al.

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For: METHOD FOR FORMING UNDERLYING INSULATION FILM

TRANSLATOR'S DECLARATION

Honorable Commissioner of Patents & Trademarks
Washington, D.C. 20231

Sir:

I, Kazuo Yoshii , residing at c/o SEIWA PATENT & LAW, Toranomon 37 Mori Bldg., 3-5-1, Toranomon Minato-ku, Tokyo 105-8423, Japan declare the following:

(1) That I know well both the Japanese and English languages;

(2) That I translated Japanese Patent Application No. 2002-97845 , filed March 29, 2002 , from the Japanese language to the English language;

(3) That the attached English translation is a true and correct translation of the aforesaid Japanese Patent Application No. 2002-97845 to the best of my knowledge and belief; and

(4) That all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001, and that such false statements may jeopardize the validity of the application or any patent issuing thereon.

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[TITLE OF THE INVENTION] Method for forming underlying insulation film

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[NAME OF DOCUMENT] SPECIFICATION

[TITLE OF THE INVENTION] Method for forming underlying insulation film

[SCOPE OF CLAIM FOR PATENT]

[Claim 1] A process for forming an underlying film, comprising: irradiating the surface of an insulating film disposed on an electronic device substrate with plasma based on a process gas comprising at least an oxygen atom-containing gas, to thereby form an underlying film at the interface between the insulating film and the electronic device substrate.

[Claim 2] A process for forming an underlying film according to claim 1, wherein the insulating film is a film comprising a high-k (high-dielectric constant) material.

[Claim 3] A process for forming an underlying film according to claim 1 or 2, wherein the plasma is plasma containing oxygen radicals.

[Claim 4] A process for forming an underlying film according to any of claims 1-3, wherein the underlying film is an oxide film.

[Claim 5] A process for forming an underlying film according to any of claims 1-4, wherein the plasma is plasma based on a plane antenna member (slot plane antenna).

[Claim 6] A process for forming an underlying film according to any of claims 1-5, which further comprises a step of annealing the high-K material film at a high temperature, after the plasma radiation.

[Claim 7] A process for forming an underlying film according to claim 6, wherein the annealing is conducted in an atmosphere

of N2, or O2.

[Claim 8] A process for forming an underlying film according to claim 6, wherein the annealing is conducted at a temperature of 600-1100 °C.

[Claim 9] An electronic device material, comprising: an electronic device substrate, an underlying film disposed on the substrate, and an insulating film disposed on the underlying film, wherein the underlying film is a film which has been formed by supplying plasma from the insulating layer side.

[Claim 10] The electronic device material according to claim 9, wherein the insulating film is a film comprising a high-k (high-dielectric constant) material.

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[Technical Field of the Invention]

The present invention relates to a process for forming an insulating film having a good interfacial property. More specifically, the present invention relates to a method of irradiating an insulating film with plasma based on a process gas comprising at least an oxygen atom-containing gas, to thereby improve the interfacial property between the insulating film and the substrate. The modification process according to the present invention is suitably usable, particularly for a so-called high-k (high-dielectric constant) material.

[0002]

[Prior Art]

In general, the present invention is widely applicable to the production of materials for electronic device such as semiconductors or semiconductor devices, and liquid crystal devices. For the convenience of explanation, however, the background art relating to semiconductor devices as an example

of the electronic devices, will be described here.

[0003]

Substrates for semiconductors or electronic device materials such as silicon have been subjected to various kinds of treatments such as formation of an oxide film, film formation by CVD (chemical vapor deposition), etc., and etching. According to the recent requirement for forming microstructures and attaining further development in the performances in the field of semiconductor devices, the demand for an insulating film having a higher performance (for example, in view of leakage current) has been increased remarkably. This is because the leakage current of a certain degree can cause a severe problem in the recent devices which have attained finer structures, and/or higher performances, even when the leakage current of such a degree have actually caused substantially no problem in the conventional devices having a lower degree of integration. Particularly, in view of the development in the mobile or portable-type electronic devices in a so-called "ubiquitous" society of recent construction (i.e., information-oriented society wherein people can use a network service, anytime and anywhere, by means of electronic devices), it is necessary to develop a low-power consumption device, and therefore the reduction in the leakage current is an extremely important issue.

[0004]

Typically, in a case where the formation of a finer structure in a high-performance silicon LSI is pursued, for example, for the purpose of developing a next-generation MOS-type transistor, there arises her performance a problem that the leakage current is increased and the resultant power consumption is also increased. Accordingly, in order to decrease the power consumption thereof while pursuing a higher performance, it is necessary to improve the transistor characteristic without increasing the gate leakage current in the MOS-type transistor.

[0005]

In order to satisfy this requirement, various techniques (for example, the modification of a silicon oxide film and the use of a silicon oxynitride film SiON) have been proposed. Among these, one useful technique is the development of an insulating film using a high-k (high-dielectric constant) material. This is because the use of such a high-k material is expected to reduce the EOT (effective oxide thickness), which is an SiO2 capacity-equivalent film thickness.

[0006]

[Problem to be Solved by the Invention]

However, when such an insulating film, which has been expected to provide a good property, is actually formed by CVD (chemical vapor deposition method) or the like, particularly in the case of the formation of an insulating film having a very high practical utility (for example, a relatively thin insulating film of about 12 A (angstrom)), a good interfacial property can be hardly obtained between the insulating film and the underlying electronic device substrate.

[0007]

One promising method for solving such a problem may be to form a very thin (for example, 10 A or less) underlying film on a substrate, and to form an insulating film on the underlying film. However, it is very difficult to form such a thin underlying film directly on an electronic device substrate by using a conventional thermal oxidation or plasma oxidation technique (the thickness of a thin film can be hardly controlled by such a technique), while controlling the film-forming rate or in-plane uniformity.

[0008]

An object of the present invention is to provide a process for forming an underlying film, which has solved the problem encountered in the prior art.

[0009]

Another object of the present invention is to provide a

process capable of forming a good underlying film at the interface between an insulating film and an electronic device substrate so as to improve the resultant transistor characteristic.

[0010]

[Means for Solving the Problem]

As a result of earnest study, the present inventors have found that, when an insulating film (for example, high-k material film) is once formed on an electronic device substrate and plasma based on a process gas comprising at least an oxygen atom-containing gas is caused to pass through the insulating film so as to form an underlying film at the insulating film-substrate interface, such a process is extremely effective in achieving the above-mentioned object, unlike the conventional technique wherein an underlying film is formed on an electronic device substrate and then an insulating film (for example, high-k material film) is formed thereon.

[0011]

The process for forming underlying insulating film according to the present invention is based on the above discovery. More specifically, the process comprises: irradiating the surface of an insulating film disposed on an electronic device substrate with plasma based on a process gas comprising at least an oxygen atom-containing gas, to thereby form an underlying film at the interface between the insulating film and the electronic device substrate.

[0012]

The present invention also provides an electronic device material, comprising: an electronic device substrate, an underlying film disposed on the substrate, and an insulating film disposed on the underlying film, wherein the underlying film is a film which has been formed by supplying plasma from the insulating layer side.

[0013]

In the process for forming an underlying film according to

the present invention having such a constitution, active plasma species (for example, oxygen reactive species) are caused to pass through the insulating film from the insulating film surface side to reach the insulating film-substrate interface, to thereby form an underlying film in the vicinity of the interface. In the present invention, the film-forming rate can be controlled (that is, the film-forming time can be controlled) easily, as compared with the case wherein an underlying film is directly formed on an electronic device substrate. Accordingly, in the present invention, it is easy to control the thickness of the underlying film and/or to improve the in-plane uniformity of the underlying film.

[00149]

[Modes for Carrying Out the Invention]

Hereinbelow, the present invention will be described in detail, with reference to the accompanying drawings as desired. In the following description, "%" and "part(s)" representing a quantitative proportion or ratio are those based on mass, unless otherwise specifically noted.

(Process for Forming Underlying Film)

[0015]

In the present invention, the surface of an insulating film disposed on an electronic device substrate is irradiated with plasma based on a process gas comprising at least an oxygen atom-containing gas, to thereby form an underlying film at the interface between the insulating film and the electronic device substrate.

(Insulating Film)

[0016]

The material for constituting the insulating film, which is usable in the present invention, is not particularly limited. In view of a practical MOS-type transistor, it is preferred to use one or at least two materials selected from the group consisting of: SiO2, SiON, each having a low dielectric constant, SiN having a relatively high dielectric

constant, and substances having a high dielectric constant, which are called a "high-k substance" as described later.

(Hi-k Material)

[0017]

The high-k material, which is usable in the present invention is not particularly limited. In view of the trend for an MOS-type transistor at a practical level, it is preferred to use those having a "k" (dielectric constant) value of 8 or more, more preferably 10 or more.

[0018]

Preferred examples of such a high-k material may include, one or at least two materials selected from the group consisting of: Al2O3, ZrO2, HfO2, Ta2O5, silicates such as ZrSiO and HfSiO, and aluminates such as ZrAlO, can be suitably used.

[0019]

(Electronic Device Substrate)

[0020]

The electronic device substrate which is usable in the present invention is not particularly limited. It is possible to use one or combination of at least two species, which are selected from the known electronic device substrates. Specific examples of the electronic device substrate may include a semiconductor material, a liquid crystal device material, etc. Specific examples of the semiconductor material may include: materials mainly comprising single-crystal silicon, and high performance CMOS, etc.

[0021]

(Underlying Film)

[0022]

The composition, thickness, stacking or lamination form, etc., of the underlying film are not particularly limited, as long as the interfacial property of the above-mentioned insulating film can be improved. In view of transistor characteristic, the underlying film may preferably be an

underlying oxide film.

[0023]

The underlying film may preferably have a thickness of about 6 to 12 A, more preferably about 6 to 8 A.

[0024]

(Process Gas Conditions)

[0025]

In the formation of the underlying film according to the present invention, the following conditions can be suitably used in view of property of the underlying film to be formed.

[0026]

Rare Gas (for example, Kr, Ar, He or Xe): from 300 to 2,000 sccm, more preferably from 1,000 to 2,000 sccm

[0027]

O2: from 1 to 500 sccm, more preferably from 10 to 300 sccm

[0028]

Temperature: from room temperature (25°C.) to 500°C., more preferably from 250 to 500°C., still more preferably from 250 to 400°C.

[0029]

Pressure: from 3 to 500 Pa, more preferably from 7 to 260 Pa

[0030]

Microwave: from 1 to 5 W/CM.sup.2, more preferably from 2 to 4 W/cm.sup.2, still more preferably from 2 to 3 W/cm.sup.2

[0031]

(Annealing)

[0032]

In the present invention, after the above-mentioned modification, the insulating film may be subjected to annealing, as desired. The conditions for the annealing are not particularly limited. In view of the transistor characteristic, a process gas containing an O2 gas and/or an N2 gas is suitably usable. Examples of the conditions, which are

suitably usable in the present invention, are described below.

[0033]

(Suitable Annealing Conditions)

[0034]

Rare Gas (for example, Kr, Ar, He or Xe): from 0 to 5,000 sccm, more preferably from 0 to 1,000 sccm

[0035]

O2: from 10 to 1,000 sccm, more preferably from 10 to 100 sccm

[0036]

N2: from 1,000 to 5,000 sccm, more preferably from 1,000 to 3,000 sccm

[0037]

Temperature: from room temperature (25°C.) to 1,050°C., more preferably from 600 to 1,050°C.

[0038]

Pressure: from 100 to 101 kPa, more preferably from 1 k to 101 kPa

[0039]

The plasma which is usable in the present invention is not particularly limited. It is preferred to use a high-density plasma having a relatively low electron temperature, because it may easily provide a uniform thin film.

[0040]

(Suitable Plasma)

[0041]

The property of the plasma which is suitably usable in the present invention are as follows.

[0042]

Electron temperature: 0.5-2.0 eV

[0043]

Density: from 1E10 to 5E12/cm.sup.3

[0044]

Uniformity of plasma density: ±10%

[0045]

(Plane Antenna Member)

[0046]

In the process for forming an electronic device material according to the present invention, plasma having a low electron temperature and a high density is formed by supplying microwave via a plane antenna member having a plurality of slots. In the present invention, the film is formed by using the plasma having such an excellent characteristic, and therefore the present invention can provide a process which accomplishes a light plasma damage, and a high reactivity at a low temperature. Further, in the present invention, as compared with a case using conventional plasma, a high-quality insulating film may easily be formed by supplying microwave via a plane antenna member.

[0047]

According to the present invention, a high-quality underlying film can be formed. Accordingly, a semiconductor device structure having an excellent characteristic may easily be formed by forming another layer (for example, an electrode layer) on the underlying film.

[0048]

(Preferred Characteristic of Underlying Film)

[0049]

According to the present invention, an underlying film having the following preferred characteristic can easily be formed.

[0050]

(Preferred Characteristic of Semiconductor Structure)

[0051]

The extent to which the process according to the present invention is applicable is not particularly limited, but the high-quality underlying film formable by the present invention can suitably be used, particularly as a gate insulator constituting an MOS structure.

[0052]

(Preferred Characteristic of MOS Semiconductor Structure)

[0053]

The very thin underlying film having a good quality, which is formable by the present invention, can suitably be used particularly as an insulating film constituting a semiconductor device (particularly, as a gate insulator constituting an MOS semiconductor structure).

[0054]

According to the present invention, an MOS semiconductor structure having the following preferred characteristic can easily be produced. When the characteristic of the insulating film which has been modified by the present invention may be evaluated, for example, by a method wherein a standard MOS semiconductor structure as described in a publication (see, Masanori Kishino and Mitsumasa Koyanagi, "VLSI Device no Butsuri (Physics of VLSI Devices)", pp. 62-63, published by Maruzen) is fabricated and the evaluation of the characteristic of the thus fabricated MOS can be used as the evaluation of the characteristic of the insulating film itself. This is because, in such a standard MOS structure, the characteristic of the insulating film constituting the MOS structure has much effect on the MOS characteristic.

[0055]

One Embodiment of Production Apparatus

[0056]

One preferred embodiment of the production process according to the present invention is described below.

[0057]

First, as an example of the structure of a semiconductor device which can be produced by the process for producing an electronic device material according to the present invention, a semiconductor device having an MOS structure having a gate insulator as the insulating film is described below, with reference to Fig. 1.

[0058]

Referring to Fig. 1(a), the reference numeral 1 in this Fig. 1(a) denotes a silicon substrate, numeral 11 denotes a field oxide film, numeral 2 denotes a gate insulator and numeral 13 denotes a gate electrode. As described above, the production process according to the present invention may provide a very thin gate insulator 2 having a good quality. Referring to Fig. 1(b), this gate insulator 2 comprises an oxide film 2 having a thickness of about 2.5 nm comprising a high-quality insulating film which has been formed at an interface with the silicon substrate 1.

[0059]

In this example, it is preferred that the high-quality oxide film 2 comprises a silicone oxide film (hereinafter referred to as "SiO2 film") which has been formed by irradiating a substrate to be treated mainly comprising Si, with a microwave through a plane antenna member having a plurality of slots in the presence of a process gas comprising O2 and a rare gas so as to generate plasma, and forming the oxide film at the surface of the substrate to be treated by using the thus generated plasma. When such SiO2 film is used, as described hereinafter, it is easy to obtain a good Si/SiO2 interfacial property (such as interfacial level), and a good gate leakage characteristic, when formed into an MOS structure.

[0060]

In the present invention, the surface of such a silicon oxide film 2 may preferably be subjected to a nitriding treatment as described above. A gate electrode 13 mainly comprising silicon (polysilocon or amouphous silicon) is further formed on the nitrided surface of the silicon oxide film 2.

[0061]

One Embodiment of Production Process

[0062]

Next, the process for producing such an electronic device material comprising a silicon oxide film 2, a nitrided surface

21, and a gate electrode 13 disposed thereon is described below.

[0085]

Fig. 3 is schematic view (schematic plan view) showing an example of the total arrangement of a semiconductor manufacturing equipment 30 for conducting the process for producing an electronic device material according to the present invention.

[0064]

As shown in Fig. 2, in a substantially central portion of the semiconductor manufacturing equipment 30, there is disposed a transportation chamber 31 for transporting a wafer W (Fig. 2). Around the transportation chamber 31, there are disposed: plasma processing units 32 and 33 for conducting various treatments on the wafer, two load lock units 34 and 35 for conducting the communication/cutoff between the respective processing chambers, a heating unit 36 for operating various heating treatments, and a heating reaction furnace 47 for conducting various heating treatments on the wafer. These units are disposed so as to surround the transportation chamber 31. Alternatively, it is also possible to provide the heating reaction furnace 47 independently and separately from the semiconductor manufacturing equipment 30.

[0065]

On the side of the load lock units 34 and 35, a preliminary cooling unit 45 and a cooling unit 46 for conducting various kinds of preliminary cooling and cooling treatments are disposed.

[0066]

In the inside of transportation chamber 31, transportation arms 37 and 38 are disposed, so as to transport the wafer W (Fig. 3) between the above-mentioned respective units 32-36.

[0067]

On the foreground side of the load lock units 34 and 35 in this figure, loader arms 41 and 42 are disposed. These loader

arms 41 and 42 can put wafer W in and out with respect to four cassettes 44 which are set on the cassette stage 43, which is disposed on the foreground side of the loader arms 41 and 42.

[0068]

In Fig. 2, as the plasma processing units 32 and 33, two plasma processing units of the same type are disposed in parallel.

[0069]

Further, it is possible to exchange both of the plasma processing units 32 and 33 with a single-chamber type CVD process unit, It is possible to set one or two of such a single-chamber type CVD process unit in the position of plasma processing units 32 and 33.

[0070]

When two plasma processing units 32 and 33 are used, it is possible that an SiO2 film is formed in the plasma processing unit 32, and the SiO2 film is nitrided in the plasma processing unit 33. Alternatively, it is also possible that the SiO2 film formation and the nitriding treatment of the SiO2 film are conducted in parallel, in the plasma processing units 32 and 33.

[0071]

One Embodiment of Plasma Processing Apparatus

[0072]

Fig. 3 is a schematic sectional view in the vertical direction showing the plasma processing unit 32 (or 33) which is usable in the film formation of the gate insulator 2.

[0073]

Referring to Fig. 3, reference numeral 50 denotes a vacuum container made of, e.g., aluminum. In the upper portion of the vacuum container 50, an opening portion 51 is formed so that the opening portion 51 is larger than a substrate (for example, wafer W). A top plate 54 in a flat cylindrical shape made of a dielectric such as quartz and aluminum nitride so as to cover the opening portion 51. In the side wall of the upper portion

of vacuum container 50 which is below the top plate 54, gas feed pipes 72 are disposed in the 16 positions, which are arranged along the circumferential direction so as to provide equal intervals therebetween. A process gas comprising at least one kind of gas selected from O2, inert gas, N2, H2, etc., can be supplied into the vicinity of the plasma region P in the vacuum container 50 from the gas feed pipes 72 evenly and uniformly.

[0074]

On the outside of the top plate 54, there is provided a radio-frequency power source, via a plane antenna member 60 having a plurality of slots, which comprises a plane antenna (SPA) made from a copper plate, for example. As the radio-frequency power source, a waveguide 63 is disposed on the top plate 54, and the waveguide 63 is connected to a microwave power supply 61 for generating microwave of 2.45 GHz, for example. The waveguide 63 comprises a combination of: a flat circular waveguide 63A, of which lower end is connected to the SPA 60; a circular waveguide 63B, one end of which is connected to the upper surface side of the circular waveguide 63A; a coaxial waveguide converter 63C connected to the upper surface side of the circular waveguide 63B; and a rectangular waveguide 63D, one end of which is connected to the side surface of the coaxial waveguide converter 63C so as to provide a right angle therebetween, and the other end of which is connected to the microwave power supply 61.

[0075]

In the present invention, UHF and microwave are inclusively referred to as "high-frequency region". That is, in the present invention, the high-frequency power to be supplied from a high-frequency power supply may be those having a frequency of not lower than 300 MHz and not higher than 2500 MHz, including UHFs having a frequency of not lower than 300 MHz, and microwaves having a frequency of not lower than 1 GHz, and plasma produced by using such high-frequency power is

referred to as "high-frequency plasma".

[0076]

In the inside of the above-mentioned circular waveguide 63B, an axial portion 62 of an electroconductive material is coaxially provided, so that one end of the axial portion 62 is connected to the central (or nearly central) portion of the SPA 60 upper surface, and the other end of the axial portion 62 is connected to the upper surface of the circular waveguide 63B, whereby the circular waveguide 63B constitutes a coaxial structure. As a result, the circular waveguide 63B is constituted so as to function as a coaxial waveguide.

[0077]

In addition, in the vacuum container 50, a stage 52 for carrying the wafer W is provided so that the stage 52 is disposed opposite to the top plate 54. The stage 52 contains a temperature control unit (not shown) disposed therein, so that the stage can function as a hot plate. Further, one end of an exhaust pipe 53 is connected to the bottom portion of the vacuum container 50, and the other end of the exhaust pipe 53 is connected to a vacuum pump 55.

[0078]

One Embodiment of SPA

[0079]

Fig. 4 is a schematic plan view showing an example of SPA 60 which is usable in an apparatus for producing an electronic device material according to the present invention.

[0080]

As shown in this Fig. 4, on the surface of the SPA 60, a plurality of slots 60a, 60a, . . . are provided in the form of concentric circles. Each slot 60a is a substantially square penetration-type groove. The adjacent slots are disposed perpendicularly to each other and arranged so as to form a shape of alphabetical "T"-type character. The length and the interval of the slot 60a arrangement are determined in accordance with the wavelength of the microwave supplied from

the microwave power supply unit 61.

[0081]

One Embodiment of Heating Reaction Furnace

[0082]

Fig. 5 is schematic sectional view in the vertical direction showing an example of the heating reaction furnace 47 which is usable in an apparatus for producing an electronic device material according to the present invention.

[0083]

As shown in Fig. 5, a processing chamber 82 of the heating reaction furnace 47 chamber is formed into an air-tight structure by using aluminum, for example. A heating mechanism and a cooling mechanism are provided in the processing chamber 82, although these mechanisms are not shown in Fig. 5.

[0084]

As shown in Fig. 5, a gas introduction pipe 83 for introducing a gas into the processing chamber 82 is connected to the upper central portion of the processing chamber 82, the inside of the processing chamber 82 communicates with the inside of the gas introduction pipe 83. In addition, the gas introduction pipe 83 is connected to a gas supply source 84. A gas is supplied from the gas supply source 84 into the gas introduction pipe 83, and the gas is introduced into the processing chamber 82 through the gas introduction pipe 83. As the gas in this case, it is possible to use one of various gas (electrode-forming gas) such as raw material for forming a gate electrode such as silane, for example. As desired, it is also possible to use an inert gas as a carrier gas.

[0085]

A gas exhaust pipe 85 for exhausting the gas in the processing chamber 82 is connected to the lower portion of the processing chamber 82, and the gas exhaust pipe 85 is connected to exhaust means (not shown) such as vacuum pump. Due to the exhaust means, the gas in the processing chamber 82 is exhausted through the gas exhaust pipe 85, and the processing

chamber 82 is maintained at a desired pressure.

[0086]

In addition, a stage 87 for carrying the wafer W is provided in the lower portion of the processing chamber 82.

[0087]

In the embodiment as shown in Fig. 5, the wafer W is carried on the stage 87 by means of an electrostatic chuck (not shown) having a diameter which is substantially the same as that of the wafer W. The stage 87 contains a heat source means (not shown) disposed therein, to thereby constitute a structure wherein the surface of the wafer W to be processed which is carried on the stage 87 can be adjusted to a desired temperature.

[0088]

The stage 87 has a mechanism which is capable of rotating the wafer w carried on the stage 87, as desired.

[0089]

In Fig. 5, an opening portion 821 for putting the wafer W in and out with respect to the processing chamber 82 is provided on the surface of the right side of the processing chamber 82 in this figure. The opening portion 821 can be opened and closed by moving a gate valve 98 vertically (up and down direction) in this figure. In Fig. 5, a transportation arm (not shown) for transporting the wafer is provided adjacent to the right side of the gate valve 98. In Fig. 5, the wafer W can be carried on the stage 87, and the wafer W after the processing thereof is transported from the processing chamber 82, as the transportation arm enters the processing chamber 82 and goes out therefrom through the medium of the opening portion 821.

[0090]

Above the stage 87, a shower head 88 as a shower member is provided. The shower head 88 is constituted so as to define the space between the stage 87 and the gas introduction pipe 83, and the shower head 88 is formed from aluminum, for

example.

[0091]

The shower head 88 is formed so that the gas exit 83a of the gas introduction pipe 83 is positioned at the upper central portion of the shower head 88. The gas is introduced into the processing chamber 82 through gas feeding holes 89 provided in the lower portion of the shower head 88.

[0092]

Embodiment of MOS Transistor Formation

[0093]

Hereinbelow, there is described a preferred example of the process wherein an insulating film comprising agate insulator 2 is formed on a wafer W.

[0094]

Fig. 6 is a flow chart showing an example of the respective steps constituting a process according to the present invention.

[0095]

Referring to Fig. 6, a field oxide film 11 (Fig. 1(a)) is formed in the previous step.

[0096]

Subsequently, a gate valve (not shown) provided at the side wall of the vacuum container 50 in the plasma processing unit 32 (Fig. 2) is opened, and the a wafer W as shown in Fig. 8, in which the field oxide film 11 has been formed on the silicon substrate 1 surface, is placed on the stage 52 (Fig. 3) by means of transportation arms 37 and 38.

[0097]

Next, the gate valve was closed so as to seal the inside of the vacuum container 50, and then the inner atmosphere therein is exhausted by the vacuum pump 55 through the exhaust pipe 53 so as to evacuate the vacuum container 50 to a predetermined degree of vacuum and a predetermined pressure in the container 50 is maintained. On the other hand, microwave, e.g., 1.80 GHz (2200 W), is generated by the microwave power

supply 61, and the microwave is guided by the waveguide so that the microwave is introduced into the vacuum container 50 via the SPA 60 and the top plate 54, whereby radio-frequency plasma is generated in the plasma region P of an upper portion in the vacuum container 50.

[0098]

Herein, the microwave is transmitted in the rectangular waveguide 63D in a rectangular mode, and is converted from the rectangular mode into a circular mode by the coaxial waveguide converter 63C. The microwave is then transmitted in the cylindrical coaxial waveguide 63B in the circular mode, and transmitted in the circular waveguide 63A in the expanded state, and is emitted from the slots 60a of the SPA 60, and penetrates the plate 54 and is introduced into the vacuum container 50. In this case, microwave is used, and accordingly high-density plasma can be generated. Further, the microwave is emitted from a large number of slots 60a of the SPA 60, and accordingly the plasma is caused to have a high density.

[0099]

The, while heating the wafer W, for example, at 400 °C by controlling the temperature of the stage 52, the first step (formation of an oxide film) is performed by introducing a rare gas such as krypton or argon, which is a process gas for the formation of an oxide film, and an O2 gas from the gas supply tube 72 at a flow rate of, for example, 2,000 sccm and 200 sccm, respectively.

[0100]

In this step, the thus introduced gas is activated (converted into plasma) by the plasma flux generated in the plasma processing unit 32, and as shown in the schematic sectional view of Fig. 8(a), the surface of the silicon substrate 1 is oxidized to form an oxide film (SiO2 film) 2. When this oxidation treatment is conducted for 40 seconds, for example, there may be formed a gate oxide film or an underlying oxide film to be used for gate underlying film (underlying SiO2

film) 2 having a thickness of 2.5 nm.

[0101]

Thereafter, a gate valve (not shown) is opened and transportation arms 37 and 38 (Fig. 2) are introduced into the vacuum container 50 so that they receive the wafer W on the stage 52. The transportation arms 37 and 38 take out the wafer W from the plasma processing unit 32, and then set the wafer on the stage in the adjacent plasma processing unit 33. Alternatively, depending on the use of the wafer, it is also possible to transport the wafer into the heating reaction furnace 47 without nitriding the gate oxide film.

[0102]

Embodiment of Nitride-Containing Layer Formation

[0103]

Subsequently, the surface of the wafer W is subjected to an surface nitridation treatment in the plasma processing unit 33, and a nitrided portion-containing layer 21 (Fig. 7(b)) is formed on the surface of the previously formed underlying oxide film (underlying SiO2) 2.

[0104]

At this surface nitridation treatment, the conditions in the vacuum container 50, for example, are set such that the wafer temperature is, for example, 400°C., and the process pressure is, for example, 66.7 Pa (500 mTorr), and an argon gas and an N2 gas are introduced into the container 50 from the gas introduction pipe at a flow rate of, for example, 1,000 sccm and 40 sccm, respectively.

[0105]

At the same time, a microwave of, for example, 2 W/cm.sup.2 is generated from a microwave power supply 61 and this microwave is guided by a wave-guide path and introduced into the vacuum container 50 through the SPA 60b and the top plate 54, whereby high-frequency plasma is generated in the plasma region P in the upper region of the vacuum container 50.

[0106]

In this step (surface nitridation), the gas introduced is converted into plasma to form nitrogen radials, and the thus formed nitrogen radials react on the SiO2 film on the upper surface of the wafer W, to thereby nitride the SiO2 film surface in a relatively short period. In this way, as shown in Fig. 7(b), the nitrogen-containing layer 21 is formed on the surface of the underlying oxide film (underlying SiO2 film) 2 on the wafer W.

[0107]

When this treatment is conducted, e.g., for 20 seconds, a gate underlying film (underlying film) having an equivalent thickness of about 2 nm may be formed.

[0108]

Embodiment of Gate Electrode Formation

[0109]

Then, a gate electrode 13 (Fig. 1(a)) is formed on the SiO2 film on the wafer W, or the underlying film which has been obtained by nitriding the underlying SiO2 film. For the purpose of the formation of the gate electrode 13, the wafer W on which the gate oxide film or gate underlying film has been formed, is taken out from the plasma processing unit 32 or 33, once into the transportation chamber 31 (Fig. 2) side, and then introduced into the heating reaction furnace 47 (step 4). In the heating reaction furnace 47, the wafer Wis heated under predetermined processing conditions, to thereby form a predetermined gate electrode 13 on the gate gate oxide film or gate underlying film.

[0110]

At this time, the treatment conditions can be selected according to the kind of the gate electrode 13 to be formed.

[0111]

More specifically, in a case where a gate electrode 13 comprising polysilicon is formed, the treatment is preformed by using, for example, SiH4 as the process gas (electrode-forming gas) under the conditions such that the pressure is from 10 to

500 Pa and the temperature is from 580 to 680°C.

[0112]

In a Case where a gate electrode 13 comprising amorphous silicon is formed, the treatment is preformed by using, for example, SIH4 as the process gas (electrode-forming gas) under the conditions such that the pressure is from 10 to 500 Pa and the temperature is from 500 to 580°C.

[0113]

(Quality of Oxide Film)

[0114]

In the above-mentioned first step, at the time of the formation of an underlying oxide film for the gate underlying film, plasma containing oxygen (O2) and rare gas is formed by supplying microwave on the wafer W mainly comprising Si through a plane antenna member (SPA) in the presence of a process gas, and by using the thus formed plasma, an oxide film is formed on the surface of the substrate to be treated, so that the oxide film can have a high quality and the film quality can be successfully controlled.

[0115]

Presumed mechanism for preferred MOS characteristics

[0116]

In addition, when the gate electrode is formed by using heat treatment in predetermined conditions in the third step, the resultant MOS-Type semiconductor structure has excellent characteristics. According to the present inventor's knowledge, the reason therefor may be presumed as follows.

[0117]

As described above, the present invention may provide an extremely thin gate insulator having a good quality. In present invention, it is possible to accomplish a good transistor characteristic (e.g., good interfacial characteristic) on the basis of the combination of the good-quality gate insulator (gate oxide film and /or gate underlying film), and a gate electrode (e.g., SiGe, amouphous silicon,

polysilicon by using CVD) to be formed thereon.

[0118]

In addition, when a cluster-type apparatus as shown in Fig. 2 is used, it is possible to avoid the exposure of the material to the atmosphere, at the interval between the formation of the gate oxide film and gate underlying film, and the formation of the gate electrode.

One embodiment of logic device formation

[0119]

Hereinbelow, there is described an embodiment of the present invention suitable for the formation of a logic device. The production process of a logic device in this embodiment is roughly carried out in the following order: "element isolation, preparation of MOS transistor, capacitance preparation, formation of interlayer insulating film and wiring".

[0120]

Among steps before the preparation of an MOS transistor including the process according to the present invention, particularly the preparation of an MOS structure deeply associated with the present invention will be explained.

[0121]

(1): Substrate

[0122]

A P-type or N-type silicon substrate having a specific resistance of 1 to 30 ?cm and plane orientation (100) is used as a substrate.

A step of element isolation such as STI or LOCOS and channel implantation have been carried out on the silicon substrate according to the purpose, and the surface of the silicon substrate, on which a gate oxide film and a gate insulating film are to be formed, has a sacrificial oxide film thereon (Fig. 8).

[0123]

(2): Cleaning before gate insulating film formation

[0124]

In general, the sacrificial oxide film and contamination elements (metals and organic matter, particles) are removed by RCA cleaning using a combination of APM (a mixed liquid composed of ammonia, aqueous hydrogen peroxide, and pure water) with HPM (a mixed liquid composed of hydrochloric acid, aqueous hydrogen peroxide, and pure water) and DHF (a mixed liquid composed of hydrofluoric acid and pure water). As desired, SPM (a mixed liquid composed of sulfuric acid and aqueous hydrogen peroxide), aqueous ozone, FPM (a mixed liquid composed of hydrofluoric acid, aqueous hydrogen peroxide, and pure water), aqueous hydrochloric acid (a mixed liquid composed of hydrochloric acid and pure water), and organic alkalis and the like are sometimes used.

[0125]

(3): Plasma treatment before base oxidation

[0126]

After the treatment in the step (2), a nitride film is formed on a substrate as a step of forming an underlying film. Wile the substrate is maintained at 600-900 °C, the substrate is rateined in an atmosphere obtained by the introduction of 1000-3000 sccm of NH3, for 1-3 min., to form a thin nitride layer (SiN layer) on the substrate surface. When the nitride layer is formed , it is possible to suppress the reaction of the substrate and HfSiO film due to heat (Fig. 9). In this step, it is also possible to use a thermal oxide film, thermal oxynitride film, an oxynitride film, oxide or nitride film formed by plasma, can be used in addition to the nitride film. However, as described above, it is difficult to form a very thin oxide film, and therefore, a technical improvement is required.

[0127]

(4): Formation of high-k gate insulating film

[0128]

A film of a high-k material is formed on the silicon substrate obtained in the step (3). As an example thereof, a

process for forming a hafnium silicate (HfSiO) film will be mainly described. Tertiary ethoxy hafnium (HTB: Hf(OC2H5)4) and silane (SiH4) gases are introduced in a flow rates of 1 sccm and 400 sccm, respectively, and the pressure is maintained at 50 Pa. The flow rate of HTB is one by a liquid mass-flow controller, and the flow rate of silane is one by a gas mass-flow controller. In this atmosphere, the silicon substrate obtained in (2) is heated at 350 °C, and reaction species (for example, Hf radicals, Si radicals, and O radicals) are allowed to react with each other on the surface of the film and consequently to form an HfSiO film. A 4nm-thick HfSiO film is formed by controlling the process conditions including process time. The film thickness can be controlled by controlling the process conditions including process time (Fig. 10).

[0129]

(5): SPA oxidation treatment

[0130]

The surface of the silicon substrate after the treatment (4) is subjected to SPA plasma oxidation treatment. As a specific example, a rare gas, and oxygen gas are supplied onto the silicon substrate heated to 400 °C at flow rates of 2000 sccm and 20 sccm, respectively, and the pressure is maintained at 67 Pa (500 mTorr). Microwaves of 2.8 W/cm2 was supplied into the atmosphere by using a plane antenna member (SPA) so as to generate plasma containing oxygen and rare gas, and the surface of the substrate obtained in step (4) is subjected to plasma oxidation treatment (Fig. 11).

[0131]

(6): Formation of polysilicon film for gate electrode

[0132]

A film of polysilicon (including amorphous silicon) is formed, as a gate electrode for an MOS transistor, by CVD on the high-k gate insulating film (including oxynitride film) formed in the step (5). The silicon substrate with the gate insulating film formed thereon is heated to a temperature

falling within the range of 500°C to 650°C, and a silicon-containing gas (for example, silane, disilane, etc.) is supplied over the substrate under a pressure of 10 to 100 Pa to form a 50 nm to 500 nm-thick polysilicon film for an electrode on the gate insulating film. In the gate electrode, silicon germanium and metals (for example, W (tungsten), Ru (ruthenium), TiN (titanium nitride), Ta (tantalum), and Mo (molybdenum)) are sometimes used as an alternative to polysilicon (Fig. 12).

[0133]

Thereafter, patterning and selective etching for a gate are performed to form an MOS capacitor (Fig. 13), and the resultant product is then subjected to ion implantation to form a source and a drain (Fig. 14). Subsequently, the dopant (for example, phosphorus (P), arsenic (As) and boron (B), etc., which have been implanted into the channel, source and drain) is activated by annealing, and then the resultant product is subjected to a wiring step as a post step by combining interlayer insulating film formation, patterning, selective etching and metal film formation. In this way, an MOS-type transistor according to this embodiment is obtained (Fig. 15). Finally, the upper part of the resultant transistor is subjected to a wiring step by using various patterns to form a circuit, to thereby complete a logic device.

[0134]

In this embodiment, Hf silicate (HfSiO film) is formed as the insulating film, but an insulating film having another composition may also e formed. As for the gate insulating film, it is possible to use one or more kinds selected from the group consisting of; SiO2, SiON, each having a low dielectric constant, which have been heretofore used, SiN having a relatively high dielectric constant, Al2O3, ZrO2, HfO2, Ta2O5, each having a high dielectric constant, which are called a high-k substance, silicates such as ZrSiO and HfSiO, and aluminates such as ZrAlO.

[0135]

In addition, only the thermal CVD process is described as a practical example of the film-formation process for the high-k substance, but an arbitrary process may be used for the film formation of the high-k substance. For example, the film formation can be also performed by plasma CVD or PVD process.

[0136]

Further, in this example, only the effect by the plasma oxidation treatment is noted, but the present invention is also applicable to, for example, plasma nitridation treatment, or a treatment comprising a combination of plasma oxidation treatment and plasma nitridation treatment, instead of the plasma oxidation treatment.

[0137]

Hereinbelow, the present invention will be described in more detail with reference to Examples.

[0138]

[EXAMPLES]

Example 1

[0139]

Fig. 16 and Fig. 17 show a change in the electrical film thickness (Teq) and in the uniformity of the electrical film thickness (range: difference between the maximum and minimum values of in-plane Teq), respectively, with respect to the oxidation time, when an oxidizing plasma processing is applied onto the HfSiO film and the oxide film formed by an SPA oxidation process. Samples as shown in Figs. 16 and 17 were produced by the following process.

[0140]

(1) Substrate

A p-type silicon substrate having a resistivity of 8 to 12 .OMEGA.cm and a plane direction of (100) was used as the substrate. On the surface of the silicon substrate, a 500 A-sacrificial oxide film was formed by a thermal oxidization process.

[0141]

(2) Pretreatment for HfSiO Film Formation

The sacrificial oxide film and contaminant factors (metals, organic materials and particles) were removed by RCA washing using a combination of APM (a mixed solution of ammonia, aqueous hydrogen peroxide and pure water), HPM (a mixed solution of hydrochloric acid, aqueous hydrogen peroxide and pure water) and DHF (a mixed solution of hydrofluoric acid and pure water). The chemical concentration ratio of the APM was NH4OH:H2O2:H2O=1:2:10 and the temperature was 60°C. The concentration ratio of the HPM was HCl:H2O2:H2O1:1:5 and the temperature was 60°C. The concentration ratio of the DHF was HF:H2O=1:9 and the temperature was 23°C. In the treatment, APM: 10 minute.fwdarw.pure water rinsing: 5 minutes.fwdarw.DHF: 23 minutes.fwdarw.pure water rinsing: 5 minutes.fwdarw.HPM: 10 minute.fwdarw.pure water rinsing: 5 minute.fwdarw.final pure water rinsing: 10 minutes were performed. Thereafter, IPA (isopropyl alcohol, 220°C.) drying was performed for 9 minutes to dry the water content on the wafer. The resulting substrate was kept at 700°C. and kept for 1 minute in an atmosphere (atmospheric pressure) where NH3 was introduced at 2,000 sccm, to thereby form a thin nitride layer (SiN layer) on the substrate surface. Due to the formation of the SiN layer, the silicon substrate and the HfSiO film can be prevented from a thermal reaction.

[0142]

(3) HfSiO Film Formation

[0143]

On the silicon substrate in the above (2), a hafnium silicate (HfSiO) film was formed. Tertiary ethoxy hafnium (HTB: Hf(OC2H5)4) and silane gas (SiH4) were introduced at 1 sccm and 400 sccm, respectively, and the pressure was kept at 50 Pa. The flow rate of HGB was the flow rate of a liquid mass-flow controller and the flow rate of silane gas was the

flow rate of a gas mass-flow controller. In this atmosphere, the silicon substrate in the above (2) was heated at 350°C. and the reactive species Hf, Si and O were reacted oh the substrate to form an HfSiO film. By controlling the process conditions including the treatment time, an HfSiO film of 4 nm was formed.

[0144]

(4) SPA Oxidation Treatment

[0145]

The silicon substrate treated in the above (3) step was then subjected to an SPA plasma oxidation treatment. On the silicone substrate heated at 400°C., a rare gas and oxygen were flown at 2,000 sccm and 200 sccm, respectively, and the pressure was kept at 67 Pa (500 mTorr). In this atmosphere, microwave of 2.8 W/cm.sup.2 was supplied through a plane antenna member (SPA) to form plasma containing oxygen and rare gas, and by using the thus formed plasma, a plasma oxidation treatment was applied onto the substrate in the above (3).

[0146]

(5) TiN Film Formation for Gate Electrode

[0147]

On the HfSiO film which had been formed through (3) and (4) steps and as a reference, on an oxide film which had been formed by performing only the oxidation treatment of (4) but omitting the HfSiO film formation of (3), a titanium nitride (TiN) film was formed as a gate electrode by a CVD process. The silicon substrate which had been treated in the above (3) and (4) steps was heated at 550°C. and under a pressure of 200 Pa, TiCl4 gas, NH3 gas and N2 gas were introduced on the substrate at 30 sccm, 100 sccm and 150 sccm, respectively, whereby a 800 A-thick TiN film for an electrode was formed on the HfSiO film.

[0148]

(6) Patterning, Gate Etching

[0149]

The TiN electrode which had been formed in the above (5) step was subjected to patterning by lithography and then, the silicon substrate was soaked in an aqueous hydrogen peroxide (H2O2) chemical solution for 3 minutes to dissolve the TiN in the non-patterned portion, to thereby form an MOS capacitor.

[0150]

Example 2

[0151]

The Cv property of the MOS capacitor which had been produced in Example 1 was evaluated. This measurement was performed by the following process. The CV property was evaluated for a capacitor having a gate electrode area of 10,000 .mu.m.sup.2. The CV property was determined by evaluating the capacitance at each voltage in the process of sweeping the gate voltage from 1 V to about -2 V at a frequency of 1 MHz. From the thus determined CV property, the electrical film thickness was calculated.

[0152]

Fig. 1 shows an electrical film thickness (Teq) when an oxidizing plasma processing is applied onto the HfSiO film and the oxide film formed by an SPA oxidation process. The abscissa indicates an oxidation treatment time and the ordinate indicates an electrical film thickness (Teq).

[0153]

As shown in Fig. 16, the reference oxide film reaches a film thickness of 25 A when the oxidation time is 20 seconds or more. As the treatment time is shorter, the reproducibility of the process becomes lower, and the control of the film thickness also becomes more difficult. Therefore, a short-time process of 20 seconds or less is not practical. This reveals that the film thickness (10 A or less) to be required as a high-k oxynitride film can be hardly obtained by the normal oxidation process as shown in the reference of Fig. 16. On the other hand, when the SPA oxidation treatment is applied to an HfSiO film as shown in Fig. 16, even if a long-time treatment

of 35 seconds or more is applied, the increase in the electrical film thickness is as small as about 10 A, based on the initial film thickness (about 16 A). Only a rare gas and an oxygen gas are used for the oxidation process, and therefore it is considered that this film thickness increase is attributable to oxygen. It is considered that the film thickness increase may include the film thickness increase from the interface and the film thickness increase in the film itself (bulk). At present, crystallization due to high-temperature annealing is known as a problem of the high-k substance including HfSiO film. This crystallization is considered to occur due to a small absolute amount of Si atoms in the film. In this meaning, the film thickness increase resulting from the mingling or mixing of oxygen into the film is unlikely the film thickness increase resulting from the insertion of O atoms into the Si--Si bonds. Also, as is known in general, the Hf--O bonds are abundantly contained. From these, the matter most greatly contributing to the film thickness increase may highly probably be the film thickness increase from the substrate, that is, the formation of an oxide film at the interface. Accordingly, it is considered that a very thin oxide film can be formed at the interface by the present invention.

[0154]

Fig. 2 shows a change in the uniformity of the electrical film thickness (range: difference between the maximum and minimum values of in-plane Teq) when an oxidizing plasma processing is applied onto the HfSiO film and the oxide film formed by the SPA oxidation process. The abscissa indicates the oxidation treatment time and the ordinate indicates the range.

[0155]

As shown in Fig. 2, in a case where the reference SPA oxide film, the range value is less changed with respect to the treatment time, but when the SPA oxidation treatment is applied

to the HfSiO film, the range becomes smaller, that is, the uniformity is further improved, as the treatment time is increased. The mechanism therefor is considered as follows. When the film thickness increase is mainly due to the formation of the oxide film at the interface as described above, a strong thickness increase effect is provided in the thin portion of film and a weak thickness increase effect is provided in the thick portion of film. Therefore, it can be considered that the non-uniformity in the film thickness is improved by applying SPA oxidation and a uniform electrical film thickness is obtained. The results of Fig. 17 can support the above-mentioned mechanism of film thickness increase in Fig. 16.

[0156]

As understood from the above, by applying plasma oxidation treatment after forming an HfSiO film, a very thin underlying film of 10 A or less can be realized, although such a thickness has been difficult to be realized by an oxidation process of a simple substance, and at the same time, an HfSiO film having a good uniformity can be formed.

[0157]

In the above Examples, only an HfSiO film produced by using the present invention is referred to, but the same effect can be obtained by applying the same treatment to other high-k substances.

[0158]

[Effect of the Invention]

As described hereinabove, the present invention can provide a process of providing a good underlying film at the interface between an insulating film and an electronic device substrate, so that the thus formed underlying film can improve the property of the insulating film.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[Fig. 1]

Fig. 1 is a schematic vertical sectional view showing an example of the semiconductor device, which can be produced by

the process for forming an underlying insulating film according to the present invention.

[Fig. 2]

Fig. 2 is a schematic vertical sectional view showing an example of the semiconductor-fabricating apparatus for practicing the process for forming an underlying insulating film according to the present invention.

[Fig. 3]

Fig. 3 is a schematic vertical sectional view showing an example of the plane antenna (SPA; sometimes also referred to as "slot plane antenna" or "SPA") plasma processing unit, which is usable in the process for forming an underlying insulating film according to the present invention.

[Fig. 4]

Fig. 4 is a schematic plan view showing an example of SPA, which is usable in the process and apparatus for forming an underlying insulating film according to the present invention.

[Fig. 5]

Fig. 5 is a schematic vertical sectional view showing an example of the heating reaction furnace unit, which is usable in the process for forming an underlying insulating film according to the present invention.

[Fig. 6]

Fig. 6 is a flow chart showing an example of the respective steps constituting a production process according to the present invention.

[Fig. 7]

Fig. 7 is schematic sectional view of the formation of a film by a process according to the present invention.

[Fig. 8]

Fig. 8 is a schematic sectional view showing an example of the silicon substrate on which a gate oxide film or gate insulating film is to be formed.

[Fig. 9]

Fig. 9 is a schematic sectional view showing an example of

the plasma processing to be effected on the surface of a substrate.

[Fig. 10]

Fig. 10 is a schematic sectional view showing an example of the formation of a high-k material film.

[Fig. 11]

Fig. 11 is a schematic sectional view showing an example of the plasma processing to be effected on a high-k material.

[Fig. 12]

Fig. 12 is a schematic sectional view showing an example of the formation of a gate electrode on a high-k material film.

[Fig. 13]

Fig. 13 is a schematic sectional view showing an example of the formation of an MOS capacitor.

[Fig. 14]

Fig. 14 is a schematic sectional view showing an example of the formation of a source and a drain by ion implantation.

[Fig. 15]

Fig. 15 is a schematic sectional view showing an example of the structure of an MOS-type transistor, which is obtainable by the present invention.

[Fig. 16]

Fig. 16 is a graph showing a change in the electrical film thickness (Teq) and uniformity in the electrical film thickness, with respect to the oxidation time, when the surface of an HfSiO film and an oxide film formed by an SPA oxidation process is subjected to an oxidizing plasma processing.

[Fig. 17]

Fig. 17 is a graph showing a change in the electrical film thickness (Teq) and uniformity in the electrical film thickness, with respect to the oxidation time, when the surface of an HfSiO film and an oxide film formed by an SPA oxidation process is subjected to an oxidizing plasma processing.